Numerical Analysis and Simulation Implementation for SVPWM Based on a New Region Segment Configuration Method

Abd Almula Gebreel, Longya Xu

Abstract— This paper proposes a new method to utilize four region segments for all sectors for a neutral point clamped (NPC) diode three-level inverter by using the space vector modulation (SVM) technique. This proposed method can be extended to more than three levels with appropriate modifications by generating appropriate inverter output voltage vectors. This paper also focuses on the analysis of the region segment configurations to realize three-level inverter operation in order to guarantee off and on equalization for all 27 switching statuses. Sectors and their regions are analyzed in order to explain the Vref movement around the original point. Segments for each region in all six sectors are configured by a new method to determine three-level inverter waveforms. There are 27 switching statuses for an NPC three-level inverter that are exploited to extract region segments, and the waveforms can be drawn manually. This study aims to explain, via simple and easy algebraic expressions, the operation of the Space Vector Pulse Width Modulation (SVPWM) on the three-level voltage inverter. The theoretical study was numerically simulated using MATLAB-SIMULINK®.

Index Terms SVPWM region segment configuration, SVPWM numerical analysis, SVPWM simulation and implementation.

1 INTRODUCTION

wenty-eight years ago, the main idea of a multilevel inverter was introduced [5],[6], which led to a lot of research being done in this area. The pulse width modulation (PWM) strategies are the most effective control for multilevel inverters. Because of the voltage stress of power switches within rated limits, thus adding to the reliability of the converter, multilevel inverters have been attracting a lot of attention in high power and voltage industry applications [2]. The switching frequency for high power application has to be less than 1 KH [4]. Even though SVM is complicated, with a large number of levels, it is the preferred method to reduce power losses by decreasing the switching frequency of the power electronics device, which can be limited by PWM. Increasing the number of output voltage converter levels leads to achieving high quality output voltages at low switching frequencies [1]. Many modulation techniques have been developed for a clamped diode multilevel inverter (CDMI).

Space vector pulse width modulation (SVPWM) is the dominant method among many modulation techniques that have been used for CDMIs [1]. The sector identification, switching-time calculation, switching-vector determination, and optimum-switching-sequence selection for the inverter voltage vectors are involved for SVPWM implementation [7]. Different aspects of the three-level NPC inverter will be discussed, including the inverter topology. The operation theory will be discussed with the aspect of SVPWM. A schematic of a three-level NPC inverter is shown in Figure 1. Each leg contains four active switches, S1 to S4, with antiparallel diodes D1 to D4. The capacitors at the DC side are used to split the DC input into two to provide a neutral point Z. The clamping diodes can be defined as the diodes connected to the neutral point, DZ1, DZ2. When switches S2 and S3 are connected, the output terminal A can be taken to the neutral through one of the clamping diodes. The voltage

applied to each of the DC capacitors is E, and it equals half of the total DC voltage.

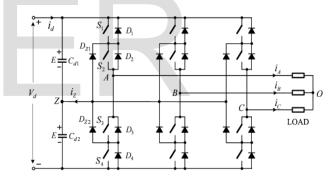


Fig. 1. Three-level NPC inverter

2 SWICHING STATES AND STATIONARY SPACE VECTORS

Switching states that are shown in Figure 1 can represent the operating status of the switches in the three-level NPC inverter. When the switching state is 1, it indicates that the upper two switches, S1 and S2, in leg A are connected and the inverter terminal voltage (the voltage for terminal A with respect to the neutral point Z) is +E, whereas the switching state of -1 denotes that the lower two switches, S3 and S4, are on and the inverter terminal voltage (the voltage for terminal A with respect to the neutral point Z) is -E. When the switching state is 0, it indicates that the inner two switches, S2 and S3, are connected and the voltage for terminal A with respect to the neutral point Z hrough the clamping diode is zero, depending on the direction of the load current. Table 1 shows the switching states for leg A. There are similar definitions of switching states for leg B and leg C.

TABLE 1											
	DEFINITION OF SWITCHING STATES										
Switching	Dev		itching ase A)	Inverter Termi-							
State	S1	S2	S3	S4	nal Voltage v_{AZ}						
1	On	On	Off	Off	Е						
0	Off	On	On	Off	0						
-1	Off	Off	On	On	- E						

The operation of each leg of a three-level inverter can be represented by one of three switching states: 1, 0, and -1. By taking all three phases into account, the inverter has a total of 27 possible switching states. Table 2 shows time calculations for vectors in sector I, and Table 3 shows the possibility of three phase-switching states that are represented by three numbers in square brackets for the inverter phases A, B, and C. The 27 switching states are shown in Figure 2. The voltage has the following four groups:

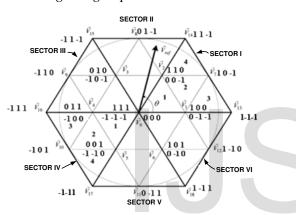


Fig. 2. Division of sectors and regions for three-level inverter

Zero vector (V0) represents three switching states: $[1 \ 1 \ 1]$, $[0 \ 0 \ 0]$, and $[-1 \ -1 \ -1]$. The magnitude of V0 is zero. The small vectors (V1 to V6), all having a magnitude of Vd/3.

TABLE 2. TIME CALCULATIONS FOR VECTORS IN SECTOR I

Region	Ta			T _b	Tc		
1	\vec{v}_1	$T_{s}\left[2m_{a}\sin\left(\frac{\pi}{3}-\theta\right)\right]$	\vec{v}_0	$T_{S}\left[1-2m_{a}\sin\!\left(\frac{\pi}{3}+\theta\right)\right]$	\vec{v}_2	$T_{S}[2m_{a}\sin\theta]$	
2	\vec{v}_1	$T_{S}[1-2m_{a}\sin\theta]$	\vec{v}_7	$T_{S}\left[2m_{a}\sin\left(\frac{\pi}{3}+\theta\right)-1\right]$	\vec{v}_2	$T_{S}\!\!\left[1\!-\!2m_{a}\sin\!\!\left(\!\frac{\pi}{3}\!-\!\theta\right)\!\right]$	
3	\vec{v}_1	$T_{S}\!\left[2-2m_{a}\sin\!\left(\frac{\pi}{3}+\theta\right)\right]$	\vec{v}_7	$T_{S}[2m_{a}\sin\theta]$	$\vec{\mathrm{v}}_{\mathrm{13}}$	$T_{S}\left[2m_{a}\sin\left(\frac{\pi}{3}-\theta\right)-1\right]$	
4	\vec{v}_{14}	$T_S[2m_a\sin\theta\!-\!1]$	\vec{v}_7	$T_{S}\left[2m_{a}\sin\left(\frac{\pi}{3}-\theta\right)\right]$	\vec{v}_2	$T_{S}\left[2-2m_{a}\sin\!\left(\frac{\pi}{3}+\theta\right)\right]$	

Each small sector has two switching states, one containing [1] and the other containing [-1]. The medium vectors (V7 to V12), whose magnitude is Vd. The large vectors (V13 to V18), all having a magnitude of V_d .

3 DETERMINING THE SECTOR AND TIME CALCULATIONS

As demonstrated in this document, the numbering for sections upper case Arabic numerals, then upper case Arabic numerals, separated by periods. Initial paragraphs after the section title are not indented. Only the initial, introductory paragraph has a drop cap.

TABLE 3. VOLTAGES AND THEIR SWITCHING STATES

	ace ctor		ing State	Vector Classification	Vector Magnitude	
V	0	[1 1 1] [-1 0		Zero vector	0	
		P-type	N-type			
V_1	V_{1P}	[100]				
-	V_1		[0 -1 -1]			
	V_{2P}	[1 1 0]			1	
V_2	V_2		[0 0 -1]			
x 7	V_{3P}	[0 1 0]		Small vector		
V_3	V_3		[-1 0 -1]	ull v	$\frac{1}{3}V_d$	
	V_{4P}	[0 1 1]		ecto	0	
V_4	V_4		[-1 0 0]	Or		
	V_{5P}	[0 0 1]				
V_5	V_5		[-1 -1 0]			
V_6	V _{6P}	[1 0 1]				
V ₆	V_6		[0 -1 0]			
V	V7	[1 () -1]	7		
V	V_8	[0]	1 -1]	Лed	_	
V	V9	[-1	10]	liun	$\frac{\sqrt{3}}{3}V_d$	
V	7 ₁₀	[-1	01]	η νε	3 "	
V	V ₁₁	[0 -	·1 1]	Medium vector		
V	7 ₁₂	[1 ·	-1 0]	r		
V	V ₁₃	[1 -	1 -1]			
V	14 / 14	[1]	1 -1]	Lai	2	
V	1 ₁₅	[-1	1 -1]	ſge	$\frac{2}{3}V_d$	
V	7 ₁₆	[-1	11]	Large vector		
V	1 ₁₇	[-1	-1 1]	tor		
V	7 ₁₈	[1 ·	·11]			

 θ is calculated, and then the sector, in which the command vector is located, is determined as follows:

If $0^{\circ} \le \theta < 60^{\circ}$, then V_{ref} will be in sector I If $60^{\circ} \le \theta < 120^{\circ}$, then V_{ref} will be in sector II If $120^{\circ} \le \theta < 180^{\circ}$, then V_{ref} will be in sector III If $180^{\circ} \le \theta < 240^{\circ}$, then V_{ref} will be in sector IV If $240^{\circ} \le \theta < 300^{\circ}$, then V_{ref} will be in sector V If $300^{\circ} \le \theta < 360^{\circ}$, then V_{ref} will be in sector VI

IJSER © 2015 http://www.ijser.org By using the same strategy that was used in the two-level inverter, the sum of the voltage multiplied by the interval of the chosen space vector equals the product of the reference voltage Vref and sampling period TS. To illustrate, when the reference voltage is located in region 2 of sector I, then the nearest vectors to the reference voltage are V1, V7, and V2, as shown in Figure 3. The next equations explain the relationship between times and voltages.

$$V_1 T_a + V_7 T_b + V_2 T_c = V_{ref} T_s$$
(1)

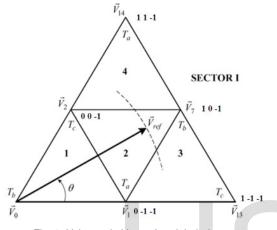


Fig. 3: Voltages in Vector I and their times

Where Ta, Tb, and Tc are the times for V1, V7, and V2, respectively. The equations for the calculation of times for sector I are given in Table 2. The times can be calculated for sectors II to VI by using the equations in Table 2 with multiple of subtracted from the actual angular displacement such that the modified angle falls into the range between zero and $\pi/3$.

The modulation index m_a can be expressed as follows:

$$m_a = \sqrt{3} \frac{V_{ref}}{V_d}$$
(2)

4 THE SWITCHING STATES BY USING SWITCHING SEQUENCES

By considering the use of sequence directions and switching transitions, shown in Figure 4, region segments for each sector can be driven. Figure 5 shows how thirteen segments for region 1 in sector I can be driven. It is obvious that region 1 sector 1 has six segments in a counterclockwise direction and seven segments in a clockwise direction to generate thirteen segments, which are given in the first row in Table 4.

These segments can be drawn manually, as can be seen in Figure 6, which gives the rotation of the voltage vector around region 1 sector I. As will be shown from the simulation results, each region will generate one step on the positive side and one step on the negative side, which will increase the number of levels in order to reduce total harmonics distortion.

TABLE 4		
THIRTEEN SEGMENTS OF REGION 1 FOR ALL S	ECT	ORS

Sector	Switching Segments												
	1	2	3	4	5	6	7	8	9	10	11	12	13
I	\vec{v}_0	\vec{v}_{1N}	\vec{V}_{2N}	$\vec{\mathrm{V}}_{\mathrm{0}}$	\vec{v}_{1P}	\vec{v}_{2P}	$\vec{\mathrm{V}}_0$	\vec{v}_{2P}	$\vec{v}_{1\text{P}}$	\vec{v}_0	\vec{v}_{2N}	\vec{v}_{1N}	\vec{V}_0
_	-1-1-1	0 -1 -1	00-1	000	100	110	111	110	100	000	00-1	0 -1 -1	-1 -1 -1
П	\vec{V}_0	\vec{V}_{2N}	\vec{V}_{3N}	$\vec{\mathrm{V}}_{\mathrm{0}}$	\vec{v}_{2P}	\vec{V}_{3P}	$\vec{\mathrm{V}}_{\mathrm{0}}$	\vec{V}_{3P}	\vec{v}_{2P}	\vec{V}_0	\vec{v}_{3N}	\vec{V}_{2N}	\vec{V}_0
11	-1 -1 - 1	00-1	-1 0 -1	000	110	010	111	010	110	000	-1 0 -1	00-1	-1 -1 -1
III	$\vec{\mathrm{V}}_{\mathrm{0}}$	\vec{V}_{3N}	\vec{V}_{4N}	$\vec{\mathrm{V}}_{\mathrm{0}}$	\vec{V}_{3P}	\vec{V}_{4P}	$\vec{\mathrm{V}}_{\mathrm{0}}$	\vec{v}_{4P}	\vec{V}_{3P}	$\vec{\mathrm{V}}_{\mathrm{0}}$	\vec{v}_{4N}	\vec{V}_{3N}	\vec{V}_0
	-1 -1 - 1	-10-1	-100	000	010	011	111	011	010	000	-100	-1 0 -1	-1 -1 -1
IV	\vec{v}_0	\vec{v}_{4N}	\vec{V}_{5N}	$\vec{\mathrm{V}}_{\mathrm{0}}$	\vec{V}_{4P}	\vec{V}_{5P}	$\vec{\mathrm{V}}_{\mathrm{0}}$	\vec{v}_{5P}	\vec{V}_{4P}	$\vec{\mathrm{V}}_{\mathrm{0}}$	\vec{V}_{5N}	\vec{v}_{4N}	\vec{V}_0
ĨV	-1 -1 - 1	-100	-1 -1 0	000	011	001	111	001	011	000	-1 -1 0	-100	-1 -1 -1
v	\vec{v}_0	\vec{V}_{5N}	$\vec{V}_{\rm 6N}$	$\vec{\mathrm{V}}_{\mathrm{0}}$	\vec{V}_{5P}	\vec{V}_{6P}	$\vec{\mathrm{V}}_{\mathrm{0}}$	\vec{v}_{6P}	\vec{V}_{5P}	$\vec{\mathrm{V}}_{\mathrm{0}}$	\vec{V}_{6N}	\vec{V}_{5N}	\vec{V}_0
v	-1 -1 - 1	-1 -1 0	0 -1 0	000	001	101	111	101	001	000	0 -1 0	-1 -1 0	-1 -1 -1
VI	\vec{v}_0	\vec{V}_{6N}	\vec{v}_{1N}	\vec{v}_0	\vec{v}_{6P}	\vec{v}_{1P}	\vec{v}_0	\vec{V}_{1P}	\vec{v}_{6P}	\vec{v}_0	\vec{v}_{1N}	\vec{v}_{6P}	\vec{V}_0
V I	-1 -1 - 1	0 -1 0	0-1-1	000	101	100	111	100	101	000	0 -1 -1	0 -1 0	-1 -1 -1

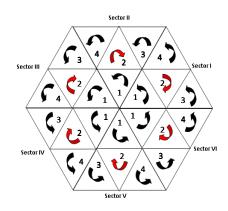


Fig. 4. Sectors, their regions, and switching sequence for three-level SVPWM inverter

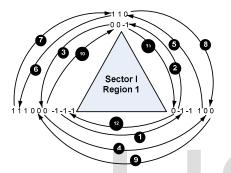
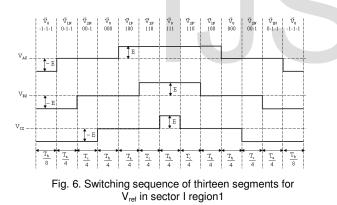


Fig. 5. Thirteen segments' configuration for region 1 sector I



By considering the vectors' expressions in Table 3 and the direction of each region in Figure 4, the same strategy can be used to determine region segments for each region in each sector. Table 4 shows thirteen segments of region 1 for each sector, Table 5 shows nine segments of region 2 for each sector, Table 6 shows seven segments of region 3 for each sector, and Table 7 shows seven segments of region 4 for each sector.

Tables 4 to 7 can be utilized to draw switching sequences for each region in each sector. Figure 5 shows thirteen segments for region 1 in sector I, Figure 7 shows nine segments for region 2 in sector I, Figure 8 shows seven segments for region 3 in sector I, and Figure 9 shows seven segments for region 4 in sector I.

TABLE 5 NINE SEGMENTS OF REGION 2 FOR ALL SECTORS

s		Switching Segments										
3	1	2	3	4	5	6	7	8	9			
I	√ _{1N}	\vec{V}_{2N}	\vec{V}_7	\vec{V}_{1P}	\vec{V}_{2P}	\vec{V}_{1P}	\vec{V}_7	\vec{v}_{2N}	\vec{V}_{1N}			
	0-1-1	00-1	10-1	100	110	100	10-1	00-1	0-1-1			
п	\vec{V}_{2N}	V _{3N}	\vec{V}_8	\vec{V}_{2P}	ν _{3Ρ}	\vec{V}_{2P}	\vec{V}_8	\vec{v}_{3N}	\vec{v}_{2N}			
	00-1	-10-1	01-1	110	010	110	01-1	-10-1	00-1			
ш	\vec{V}_{3N}	\vec{V}_{4N}	\vec{V}_9	\vec{V}_{3P}	\vec{V}_{4P}	\vec{V}_{3P}	\vec{V}_9	\vec{V}_{4N}	\vec{v}_{3N}			
	-10-1	-100	-110	010	011	010	-110	-100	-10-1			
IV	\vec{V}_{4N}	\vec{V}_{5N}	\vec{V}_{10}	\vec{V}_{4P}	\vec{V}_{5P}	\vec{V}_{4P}	\vec{V}_{10}	\vec{V}_{5N}	\vec{V}_{4N}			
	-100	-1-10	-101	011	001	011	-101	-1-10	-100			
v	\vec{V}_{5N}	V _{6N}	\vec{v}_{11}	\vec{V}_{5P}	₿ V _{6P}	\vec{V}_{5P}	\vec{v}_{11}	\vec{V}_{6N}	\vec{V}_{5N}			
	-1-10	0-10	0-11	001	101	001	0-11	0-10	-1-10			
VI	V _{6N}	\vec{v}_{1N}	\vec{v}_{12}	\vec{V}_{6P}	\vec{v}_{1P}	\vec{v}_{6P}	\vec{V}_{12}	\vec{v}_{1N}	\vec{V}_{6N}			
	0-10	0-1-1	1-10	101	100	101	1-10	0-1-1	0-10			

 TABLE 6

 NINE SEGMENTS OF REGION 3 FOR ALL SECTORS

Switching Segments											
S	1	2	3	4	5	6	7				
Ι	\vec{v}_{lN}	\vec{V}_{13}	\vec{V}_7	\vec{V}_{1P}	\vec{V}_7	\vec{v}_{13}	\vec{V}_{lN}				
	0-1-1	1-1-1	10-1	100	10-1	1-1-1	0-1-1				
Π	\vec{V}_{2N}	\vec{V}_{14}	\vec{V}_8	\vec{v}_{2P}	\vec{V}_8	\vec{v}_{14}	\vec{v}_{2N}				
	00-1	11-1	01-1	110	01-1	11-1	00-1				
II I	\vec{V}_{3N}	\vec{V}_{15}	\vec{V}_9	\vec{V}_{3P}	\vec{V}_9	\vec{V}_{15}	\vec{V}_{3N}				
1	-10-1	-11-1	-110	010	-110	-11-1	-10-1				
I V	\vec{V}_{4N}	\vec{v}_{16}	\vec{V}_{10}	\vec{v}_{4P}	\vec{V}_{10}	\vec{V}_{16}	\vec{v}_{4N}				
v	-100	-111	-101	011	-101	-111	-100				
v	\vec{V}_{5N}	\vec{v}_{17}	\vec{v}_{11}	\vec{V}_{5P}	\vec{V}_{11}	\vec{V}_{17}	\vec{V}_{5N}				
	-1-10	-1-11	0-11	001	0-11	-1-11	-1-10				
V V I	V _{6N}	\vec{V}_{18}	\vec{v}_{12}	\vec{V}_{6P}	\vec{v}_{12}	\vec{V}_{18}	\vec{V}_{6N}				
1	0-10	1-11	1-10	101	1-10	1-11	0-10				

 TABLE 7

 NINE SEGMENTS OF REGION 4 FOR ALL SECTORS

	Switching Segments											
S	1	2	3	4	5	6	7					
I	\vec{V}_{2N}	\vec{V}_7	\vec{v}_{14}	\vec{V}_{2P}	\vec{v}_{14}	\vec{V}_7	\vec{V}_{2N}					
	00-1	10-1	11-1	110	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	00-1						
п	\vec{V}_{3N}	\vec{V}_8	\vec{V}_{15}	\vec{V}_{3P}	\vec{V}_{15}	\vec{V}_8	\vec{V}_{3N}					
	-10-1	01-1	-11-1	010	-11-1	01-1	-10-1					
III	\vec{V}_{4N}	\vec{V}_9	\vec{v}_{16}	\vec{V}_{4P}	\vec{v}_{16}	\vec{V}_9	$\vec{\mathrm{V}}_{4\mathrm{N}}$					
	-100	-110	-111	011	-111	-110	-100					
IV	\vec{V}_{5N}	\vec{V}_{10}	\vec{V}_{17}	\vec{V}_{5P}	\vec{V}_{17}	\vec{V}_{10}	\vec{V}_{5N}					
	-1-10	-101	-1-11	001	-1-11	-101	-1-10					
v	\vec{v}_{6N}	$\vec{v}_{\!11}$	\vec{V}_{18}	\vec{V}_{6P}	\vec{V}_{18}	\vec{v}_{11}	\vec{v}_{6N}					
	0-10	0-11	1-11	101	1-11	0-11	0-10					
VI	\vec{V}_{1N}	\vec{v}_{12}	\vec{v}_{13}	\vec{V}_{1P}	\vec{v}_{13}	\vec{v}_{12}	\vec{V}_{lN}					
	0-1-1	1-10	1-1-1	100	1-1-1	1-10	0-1-1					

Tables 4 to 7 can be utilized to draw switching sequences for each region in each sector. Figure 5 shows thirteen segments for region 1 in sector I, Figure 7 shows nine segments for region 2 in sector I, Figure 8 shows seven segments for region 3 in sector I, and Figure 9 shows seven segments for region 4 in sector I. Thirteen segments for region 1 in sectors II to VI, nine segments for region 2 in sectors II to VI, seven segments for region 3 in sectors II to VI, and seven segments for region 4 in sectors II to VI can be drawn, as the same way had been used for sector I.

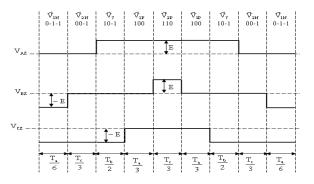


Fig. 7. Switching sequence of nine segments for $V_{\mbox{\scriptsize ref}}$ in sector I region 2

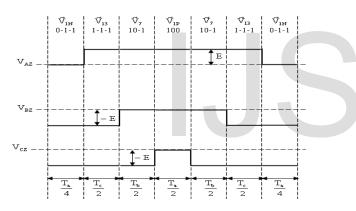


Fig. 8. Switching sequence of seven segments for V_{ref} in sector I region 3

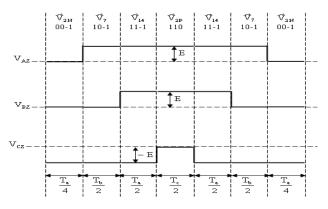


Fig. 9. Switching sequence of seven segments for $V_{\mbox{\tiny ref}}$ in sector I region 4

5 SIMULATION RESULTS

The specifications system feeds a passive load for R=1 Ω and L=0.01H. A switching frequency of 2.5kHz was used in the model. The DC link voltage of the clamped diode three-

level inverters was taken as 700V. Simulation results were taken for the specifications system above. The inverter was simulated and improved by employing switching status in Tables 4, 5, 6, and 7 for SVPWM control. The simulation results of three phase current, line to neutral voltage, and line to line voltage by MATLAB were recorded. Figures 10 to 12 show three phase voltages, three phase to phase voltages, and three phase current, respectively.

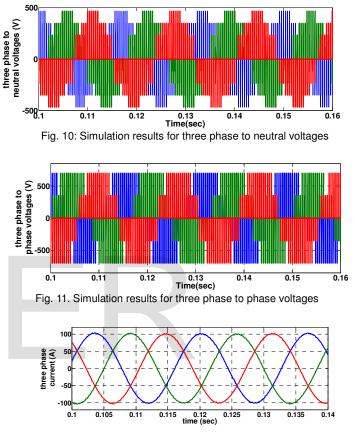


Fig. 12. Simulation results for three phase output current

Figures 13 and 14 show the voltage Va (phase voltage) and the voltage Vab (phase-to-phase voltage). As mentioned before, because of following a control based on a new region segment configuration method, the number of voltage steps can be increased by one on the positive side and one on the negative side.

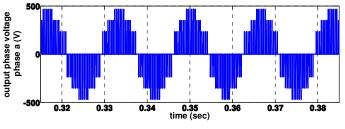


Fig. 13. Simulation results for output voltage phase for phase a

To verify the efficiency and quality of the proposed SVPWM using all region segments in each sector, some transi-

ent tests have been carried out. For the first test, step down was executed in the modulation index from 1 to 0.5 at time 20*(1/60) and then step up was executed in the modulation index from 0.5 to 1 at time (23*(1/60)). It is interesting to show the impact on phase to neutral voltage and current and phase to phase voltage.

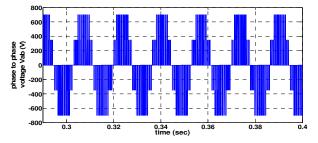


Fig. 14. Simulation results for output voltage phase to phase voltage (Vab)

Figures 15 to 17 show the response of phase to neutral voltage, phase to phase voltage, and phase current, respectively. For step down for the modulation index, it is obvious that the maximum values for all quantities are decreased in order to follow the new reference, which is 0.5. The number of levels for phase to neutral levels was decreased from 7 to 5 levels per cycle as expected and as can be seen in Figure 15. Phase to phase voltage levels were decreased from 5 to 3 levels per cycle as expected and as can be seen in Figure 16. Figure 17 shows the response of the output phase current, which is really fast and reaches the expected value, and it was decreased smoothly without any oscillations.

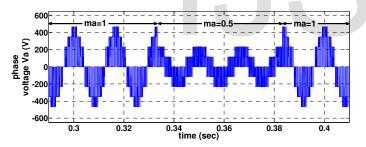


Fig. 15. Simulation results for output phase to neutral voltage response for step down and up in the modulation index

For step up for the modulation index, it is obvious that the maximum values for all quantities are increased to the original values in order to follow the new reference, which is 1. The number of levels for phase to neutral voltage levels was recovered again from 5 to 7 levels per cycle as expected and as can be seen in Figure 13.

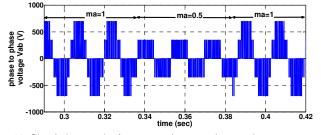


Fig. 16. Simulation results for output phase to phase voltage response for step down and up in the modulation index

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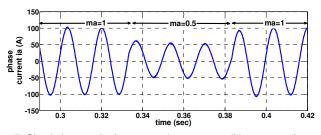


Fig. 17. Simulation results for output phase current (i_a) response for step down and up in the modulation index

Phase to phase voltage levels were also recovered again from 3 to 5 levels per cycle as expected and as can be seen in Figure 14. Again, Figure 15 shows the response of the output phase current, which is really fast and reaches the expected value, and it was increased smoothly to the original value without any oscillations. The recovery time is almost zero seconds, comparable with the other type of multilevel inverter using the same procedure. The stability should not be affected by the switching frequency. In Figures 13 and 14, the output phase to neutral voltage and phase to phase voltage response is very fast, and the current waveform in Figure 15 is very smooth due to the high equivalent switching frequency that was used by utilizing all switching cases in Tables 4 to 7. Figures 13 to 15 prove the efficiency of the proposed SVPWM using all region segments in each sector where all the quantities do not contain any oscillations.

For the second test for the proposed SVPWM using all region segments in each sector, a step load was executed at $(20^*(1/60))$ seconds, driving from the inverter the double of the current. It is interesting to show the impacts on all the variables of the inverter, including phase current, phase voltage, and phase to phase voltage. Figure 18 shows the response of the phase to neutral output voltage. Even though the load was increased 100%, the output phase to neutral voltage is still stable without any disturbance or oscillations, which leads to phase to phase output voltage not having any impacts, as can be seen in Figure 19.

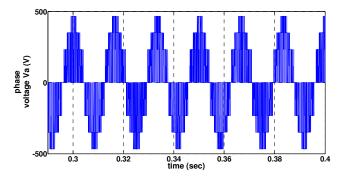


Fig. 18. Simulation results for output phase to neutral voltage response for a load step

Figure 20 shows the response of the output current. Since the load was increased 100%, the peak value is increased from 100A to 200A, which remains without significant disturbances, and the recovery time is almost one cycle (0.01667 seconds), which gives an indicator that the current has fast response.

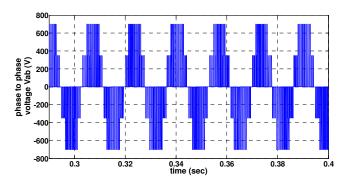


Fig. 19. Simulation results for output phase to phase voltage response for a load step.

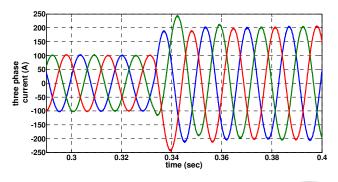


Fig. 20. Simulation results for output three phase current response for a load step.

6 CONCLUSION

This paper provides a comprehensive analysis on the threelevel diode clamped inverter. A number of issues were investigated, including the inverter configuration, operating principle, and space vector and modulation (SVM) techniques. The performance of the three-phase three-level twelve-switch inverter has been explained and improved by employing all switching statuses for the SVPWM control scheme. The use of three-level inverters reduces the harmonic components of the output voltage by increasing the number of levels compared with the two-level inverter at the same switching frequency. The switching sequence for each region in each sector has been explained in details, which were utilized in the designed and implemented diode clamped three-level inverter to realize the requirements and feed the R-L load by the required values of voltage and frequency. Also, some derivations, such as thirteen segments of region 1 for each sector, nine segments of region 2 for each sector, and seven segments of region 3 for each sector for the three-level inverter, which have never been mentioned before, were derived, and the switching sequence for each region in each sector was determined. Simulation results with different tests for the proposed technique were also presented. Step down and step up tests in the modulation index, as well as a load step test, were simulated. All quantities including phase current, phase voltage, and phase to phase voltage did not contain any oscillations with the two tests used. The transient responses for the step load and step modulation index were fast and did not lead to system instability for all quantities.

REFERENCES

- T. Nathenas, G. Adamidis, "A new approach for SVPWM of a three-level inverter-induction motor fed-neutral point balancing algorithm," Simulation Modeling Practice and Theory, Vol. 29, pp. 1-17, Dec. 2012.
- [2] K. K. Kumar, S. Jain, "A multilevel Voltage Source Inverter (VSI) to maximize the number of levels in output waveform," *Simulation Modeling Practice and Theory*, Vol. 44, No. 1, pp. 25-36, Jan. 2013.
- [3] C. Bharatiraja, S. Jeevananthan, R. Latha, S. S. Dash, "A Space Pulse Width Modulation for DC Link Voltage Balancing in Diode-Clamped Multilevel Inverter," AASRI Procedia, Vol. 3, pp. 133-140, 2012.
- [4] J. Suh, C. Choi, D. Hyun, "A New Simplified Space Pulse-Vector PWM Method for Three-Level Inverter," *IEEE Transactions on Power Electronics*, Vol. 16, pp. 545-550, Jul. 2001.
- [5] A. Nabae, I. Takahashi, H. Akagi, "A New Neutral-Point-Clamped PWM Inverter," *IEEE Transactions on Industry Applications*, Vol. 1A-17, No., pp. 548-523, Oct. 1981.
- [6] J. Lai, F. Z. Peng, "Multilevel Converters-A New breed of Power Converters," IEEE Industry Applications Conference, Vol. 3, pp. 2348-2356, Oct. 1995.
- [7] A. Mohamed, A. Gopinath, M. R. Baiju, "A Simple Space Vector PWM Generation Scheme for Any General n-Level Inverter," *IEEE Transaction on Industrial Electronics*, Vol. 56, No. 5, pp. 1649-1656, May 2009.
- [8] J. F. Khan, S. M. A. Bhuiyan, K. M. Rahman, G. V. Murphy, "Space vector PWM for a two-phase VSI," *International Journal of Electrical Power & Energy* Systems, Vol. 51, pp. 265-277, Oct 2013.
- [9] M. V. Rajkumar, P. S. Manoharan, A. Ravi, "Simulation and an experimental investigation of SVPWM technique on a multilevel voltage source inverter for photovoltaic systems," *International Journal of Electrical Power & Energy Systems*, Vol. 52, pp. 116-131, Nov. 2013.
- [10] A. K. Gupta, A. M. Khambadkone, "A Space Vector PWM Scheme for Multilevel Inverters Based on Two-Level Space Vector PWM," *IEEE Transaction on Industrial Electronics*, Vol. 53, No. 5, pp 1631-1639, Oct 2006.
- [11] C. Bharatiraja, S. Jeevananthan, R. Latha, "FPGA based practical implementation of NPC-MLI with SVPWM for an autonomous operation PV system with capacitor balancing," *International Journal of Electrical Power & Energy Systems*, Vol. 61, No. 1, pp. 489-509, Oct. 2014.
- [12] D. G. Holmes, "The Significance of Zero Space Vector Placement for Carrier-Based PWM Schemes," *IEEE Transaction on Industry Applications*, Vol. 32, No. 5, pp 2451-2458, Oct 1996.
- [13] G. Chen, J. Kang, J. Zhao, "Numeric analysis and simulation of space vector pulse width modulation," *Advances in Engineering Software*, Vol. 65, pp. 60-65, Nov. 2013.
- [14] J. Zhou, X. Wu, Y. Geng, P. Dai, "Simulation Research on a SVPWM Control Algorithm for a Four-Leg Active Power Filter," *Journal of China University of Mining and Technology*, Vol. 17, No. 4, pp. 590-594, Dec. 2007.
- [15] N. Moungkhum, W. Subsingha, "Voltage Control by DQ Frame Technique of SVPWM AC-DC Converter," *Energy Procedia*, Vol. 34, pp. 341-350, 2007.
- [16] C. Bharatiraja, S. Jeevananthan, R. Latha, S. S. Dash, "A Space Vector Pulse Width Modulation Approach for DC Link Voltage Balancing in Diode-Clamped Multilevel Inverter," *AASRI Procedia*, Vol. 3, pp. 133-140, 2012.
- [17] A. G. Gebreel, "simulation and implementation of two level and three-level inverters by matlab and rt-lab," *master thesis , ohio State university*, 2011.
- [18] J. Zhang, "High Performance Control of a Three-Level IGBT Inverter Fed AC Drive," Industry Applications Conference, Vol. 1, pp. 22-28, Oct. 1995.
- [19] J. Itoh, Y. Noge, and T Adachi, "A Novel Five-level Three-phase PWM Rectifier using 12 Switches," *IEEE Transaction On Power Electronics*, Vol. 26, No. 8, pp. 3100-3107, Aug. 2011.
- [20] A. Michael, N. Devarajan, "FPGA Implementation of Multilevel Space Vector PWM Algorithms," *International Journal of Engineering and Technology*, Vol. 1, pp. 709-716, Agu. 2009.
- [21] N. F. Mailah, "Neutral-Point-Clamped Multilevel Inverter Using Space Vector Modulation," European Journal of Scientific Research, Vol.28 No.1, pp. 82-91, 2009.

- [22] S. Wen-xiang, Y. Gang, C. Chen, "Control Method of Three-level Neutralpoint-clamped Inverter Based on Voltage Vector Diagram Partition," J. Shanghai Jiaotong Univ. (Sci.), 13(4), pp. 457–461, 2008.
- [23] X. Xie, Q. Song, G. Yan, W. Liu, "MATLAB-based Simulation of Three-level PWM Inverter-fed Motor Speed Control System," *Applied Power Electronics Conference and Exposition*, Vol. 2, pp. 1105-1110, Feb. 2003.
- [24] A. Kocalmış, S. Sünter, "Simulation of a Space Vector PWM Controller for a Three-Level Voltage-Fed Inverter Motor Drive," IEEE Industrial Electronics, IECON 2006 - 32nd Annual Conference on, pp. 1915-1920, 2006.
- [25] J. Chang, J. Hu, F. Z. Peng, "Modular, Pinched DC-Link and Soft Commutated Three-Level Inverter," *Power Electronics Specialists Conference*, Vol.2, pp. 1065-1070, Jul. 1999.
- [26] H. Djeghloud, H. Benalla, "Space Vector Pulse Width Modulation Applied to the Three-Level Voltage Inverter," *Electrotechnic's Laboratory of Constantine*, *Mentouri-Constantine University*, Constantine 25000, Algeria.
- [27] V.T. Somasekhar, K. Gopakumar, "Three-level inverter configuration cascading Two Two-Level Inverters," *Electric Power Applications, IEE Proceedings*, Vol.150, pp. 245-254, May 2003.



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